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Tae Min Kim; Hyundong Shin; Jae Hong Lee;

Vehicular Technology Conference, 2002. Proceedings. VTC 2002-Fall. 2002 IEEE 56th , Volume: 4 , 24-28 Sept. 2002

Pages:2168 - 2171 vol.4

[\[Abstract\]](#) [\[PDF Full-Text \(344 KB\)\]](#) IEEE CNF

2 **Fast parallel CRC algorithm and implementation on a configurable processor**

Ji, H.M.; Killian, E.;

Communications, 2002. ICC 2002. IEEE International Conference on , Volume: 3 , 28 April-2 May 2002

Pages:1813 - 1817 vol.3

[\[Abstract\]](#) [\[PDF Full-Text \(410 KB\)\]](#) IEEE CNF

3 **A fast CRC implementation on FPGA using a pipelined architecture for the polynomial division**

Monteiro, F.; Dandache, A.; M'sir, A.; Lepley, B.;

Electronics, Circuits and Systems, 2001. ICECS 2001. The 8th IEEE International Conference on , Volume: 3 , 2-5 Sept. 2001

Pages:1231 - 1234 vol.3

[\[Abstract\]](#) [\[PDF Full-Text \(208 KB\)\]](#) IEEE CNF

4 **Parallel CRC realization**

Campobello, G.; Patane, G.; Russo, M.;

Computers, IEEE Transactions on , Volume: 52 , Issue: 10 , Oct. 2003

Pages:1312 - 1319

[\[Abstract\]](#) [\[PDF Full-Text \(413 KB\)\]](#) IEEE JNL

5 **CRC-16 polynomials optimized for applications using self-synchronous scramblers**

Gorshe, S.S.;

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Electronics, Circuits and Systems, 2003. ICECS 2003. Proceedings of the 2003 10th IEEE International Conference on , Volume: 3 , 14-17 Dec. 2003

Pages:1002 - 1005 Vol.3

[\[Abstract\]](#)[\[PDF Full-Text \(1411 KB\)\]](#)**IEEE CNF**

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1 Finding BCH error locator polynomials in one step

Cooper, A.B.;

Electronics Letters, Volume: 27, Issue: 22, 24 Oct. 1991

Pages:2090 - 2091

[\[Abstract\]](#) [\[PDF Full-Text \(140 KB\)\]](#) **IEEE JNL**

2 A fast algorithm for the decoding of binary BCH codes

Penzhorn, W.T.;

Communications and Signal Processing, 1993., Proceedings of the 1993 IEEE South African Symposium on, 6 Aug. 1993

Pages:63 - 64

[\[Abstract\]](#) [\[PDF Full-Text \(104 KB\)\]](#) **IEEE CNF**

3 On acceptance criterion for efficient successive errors-and-erasures decoding of Reed-Solomon and BCH codes

Kamiya, N.;

Information Theory, IEEE Transactions on, Volume: 43, Issue: 5, Sept. 1997

Pages:1477 - 1488

[\[Abstract\]](#) [\[PDF Full-Text \(728 KB\)\]](#) **IEEE JNL**

4 A new look at double error correcting BCH codes

Crepeau, P.J.;

Military Communications Conference, 1996. MILCOM '96, Conference Proceedings, IEEE, Volume: 2, 21-24 Oct. 1996

Pages:426 - 430 vol.2

[\[Abstract\]](#) [\[PDF Full-Text \(412 KB\)\]](#) **IEEE CNF**

5 Studying the locator polynomials of minimum weight codewords of BCH codes

Augot, D.; Charpin, P.; Sendrier, N.;

Information Theory, IEEE Transactions on, Volume: 38, Issue: 3, May 1992

Pages:960 - 973

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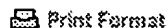
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1 **FASTBUS simulation tools**

Dean, T.D.; Haney, M.J.;

Nuclear Science, IEEE Transactions on , Volume: 39 , Issue: 4 , Aug 1992

Pages:910 - 914

[\[Abstract\]](#) [\[PDF Full-Text \(424 KB\)\]](#) **IEEE JNL**

2 **Implementation of a state space controller in a FPGA**

Garberg, B.; Sohlberg, B.;

Electrotechnical Conference, 1998. MELECON 98., 9th Mediterranean , Volume:

1 , 18-20 May 1998

Pages:566 - 569 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(256 KB\)\]](#) **IEEE CNF**

3 **FASTBUS simulation tools**

Dean, T.D.; Haney, M.J.;

Nuclear Science Symposium and Medical Imaging Conference, 1991., Conference

Record of the 1991 IEEE , 2-9 Nov. 1991

Pages:918 - 922 vol.2

[\[Abstract\]](#) [\[PDF Full-Text \(376 KB\)\]](#) **IEEE CNF**